REMARKS

Objections to the Drawings

The objections to the drawings are overcome by modification of the specification. The numeral "10" has been eliminated since it is a reference for the whole figure which is adequately referenced in the "Brief Description of the Drawings". Numeral "14′" is used as a reference numeral in Figure 1 to identify the "DUT". Accordingly, in line 1 of page 2, of the specification "14" has been changed to "14′". In addition, a reference to REGs 138 and 142 has been added to the specification.

Objections to the Abstract

The abstract has been shortened to one paragraph in light of the Examiner's remarks.

Claim Rejection under 35 USC 112 (first paragraph)

Applicant identifies "a flat pseudo random pattern", on lines 18 to 22 of page 2, as a pattern of the type produced by an LFSR. The Koenemann patent, starting on line 65 of column 1, discusses "flat random patterns". Those skilled in the art are knowledgeable of this type of pseudo random pattern and therefore know what is referred to as "flat pseudo random pattern", as evidenced by the Examiner's comments on page 5 of his action.

Rejection Under 35 USC 102 (second paragraph)

Claim 1 has been amended in light of the Examiner's comments to provide proper antecedent basis for terms in the claim.

Rejections Under 35 USC 102 and 103

Original claims 1, 2, 4, 7, 8 and 9 were rejected under 35 USC 102 (b) as anticipated by the Eichelberger et al., U.S. Pat. 4,687,988 while original claims 3, 5 and 6 were rejected on the basis of the above mentioned Eichelberger patent in view of Koenerman et al., U.S. Pat. 5,612,963.

In accordance with the present invention, test apparatus provides both flat pseudo random test patterns in combination with weighted pseudo random test patterns so that the weight applied to every latch in the LSSD chain can be changed on every cycle. This apparatus fully integrates on-chip weighted pattern generation with either internal or external weight selection. With WRP test technology, the WRP patterns are generated by the tester either externally or internally to the DUT and loaded via the shift register inputs (SRIs or WPIs) into the chip's shift register latches (SRLs). A test (or LSSD tester loop sequence) includes loading the SRLs in the SR chains with a WRP, pulsing the appropriate clocks, and unloading the responses captured in the SRLs into the multiple input signature register (MISR). Each test can then be applied multiple times for each weight set, with the weight-set assigning a weight factor or probability to each SRL.

With the above arrangement, only specific subsets of SRLs of the LSSD chain need to be weighted with each weight-set. The remaining SRLs, those not included in the weighted subset, can be loaded with "flat" pseudo-random patterns generated by the built-in LFSR. Furthermore, multiple sets of weights and associated with multiple subsets of SRLs and also be used. From "none" to "all" the latches in the array can be modified on each scan shift cycle.

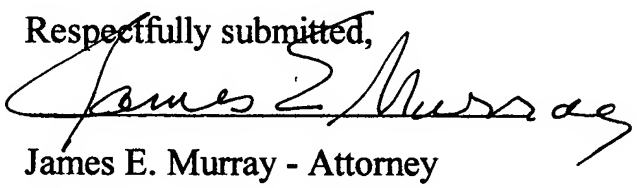
With respect to the rejection of claims under 35 USC 102, the Examiner points out that Eichelberger does not explicitly teach use of BIST technology where the weighting circuitry is part of the integrated circuit under test. Independent claim 1 calls for "an integrated circuit" with "self test circuits comprising" the recited elements of the claim. Similarly, independent claim 8 claims "a method of testing an integrated circuit with self test circuits on the integrated circuit". Therefore, Eichelberger does not identically disclose the invention claimed in the claims as required by 35 USC 102. As for the rejection of claims under 35 USC 103, it would not be obvious to combine the teachings of the Eichelberger and Koenemann patents, as proposed by the Examiner. The Koenemann patent particularly points out in column 2, beginning on line 50 that it "becomes prohibitively expensive to implement weighted random pattern generators ... on chip as the weight factor F_j increases." In view of this problem, those skilled in the art would be unlikely to incorporate multiple copies of the complex weighting circuit of Figure 3 of Eichelberger onto the chip, as proposed by the Examiner. Further, as far as this applicant's attorney sees, neither Figure 4 of Eichelberger or Koenemann contain storage elements between the weight generators and the scan chain, which elements are addressed through a decoder which enables selective entry of signals from the weight circuits on a SRL by SRL basis in each of the scan chain. As pointed out

above, applicant uses this arrangement to enter weighted pseudo-random patterns into only specific subsets of SRLs in a LSSD chain while the remaining SRLs in the chain can be loaded with flat pseudo-random patterns.

For the above reasons, the claims of the application are patentable over the applied references. As amended, independent claim 1 recites a selection circuit for entering either a flat or weighted pseudo-random pattern into the scan chain on an SRL by SRL basis. Claim 8 calls for a selection circuit providing flat or weighted pseudo-random patterns to scan chains on a shift register latch by shift register latch basis. The dependent claims add additional limitations that further distinguish them from the prior art combination cited by the Examiner.

For the above reasons, it is respectfully submitted that all claims are allowable, and therefore it is requested that the application be reconsidered, allowed and passed to issue.

Respectfully submitted,



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